Remarks

It is observed that the Examiner rejected claims 1-16 as containing subject-matter which was not described in the specification.

In particular, the Examiner said that:

a) it is not clear how the components connected as described in the specification and figures 2-3 results in the complex signal converted from the real signal;
b) the function of the first adder is not clear;
c) the operation of the selector is not clear;
d) the function of the multipliers is not clear.

It is submitted the following.
In addition to the comments already presented by the applicant in the reply to the first Office Action, the applicant submits the following explanations as required by the Examiner.
As to the Examiner's question about how the components connected as described in the specification and figures 2-3 result in the complex signal converted from the real signal, the applicant submits the following explanation by means of waveform diagrams obtained by Labview tool from National Instruments:

The first adder is an adder which performs a sum operation such that Vout(t) = Input(t) + Osc(t), with Input being a signal 1, Osc being a signal from oscillator 7 and Vout being signal 9.

The selector 10 is a device which sends In signal 9 to output A when Sel signal is 1 or to output B when Sel signal is 2; outputs A and B are zero when Sel signal is 0;
or a device which has

OutA(t) = In(t), OutB(t) = 0 when Sel(t) is 1
OutB(t) = In(t), OutA(t) = 0 when Sel(t) is 2
OutA(t) = 0, OutB(t) = 0 when Sel(t) is 0.

The selector sends the signal alternately

- for a period of 4 times the center frequency

or

-for a period of 1/4 times the period of the center frequency.

The period of conduction to I and Q being identical and being the repetition rate of the Sel signal 2 time the center frequency.

The Multipliers 14 and 15 are multipliers or devices which perfrom a multiply operation such that Vout(t) = Vin(t) * Vmult(t).

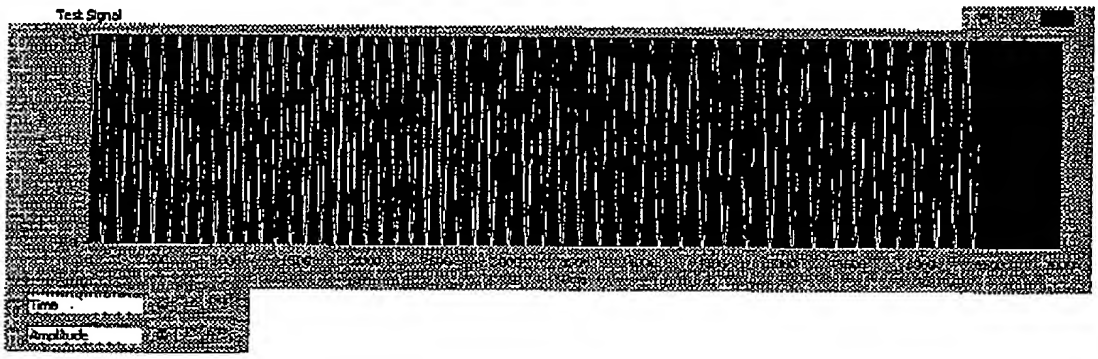
Mixer is a term used in Rf to perform the multiplication function but while all multipliers are mixers, not all mixers are multipliers. As this process can be implemented in digital or analog domain, we prefer the term multiplier.

A simulation is carried out with Labview tool from National Instruments.

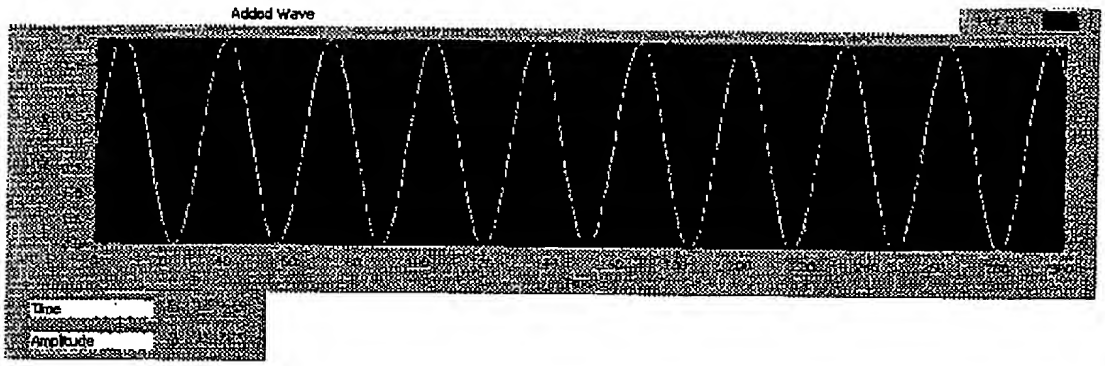
The block diagram is file brev_quad..vi (it is herewith enclosed)

The left block generates a signal which is frequency modulated.

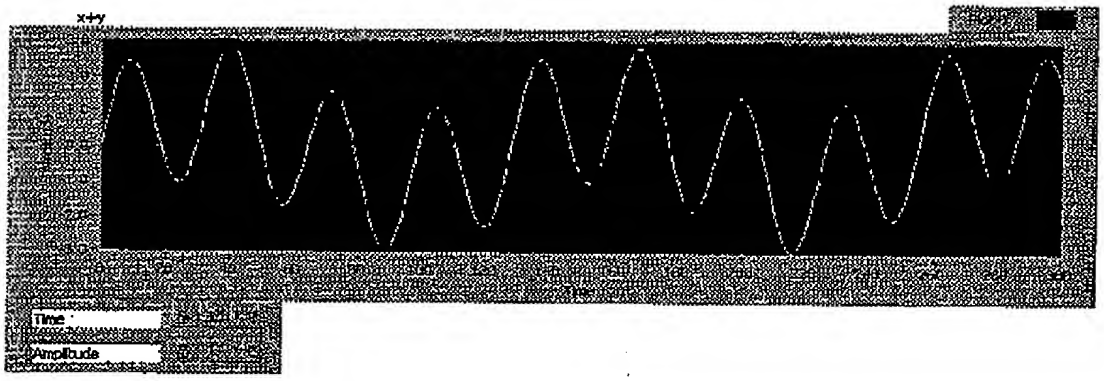
The signal is named Test Signal



To this signal, which has a center frequency period of 128 samples, a signal with period of 32 samples is added.



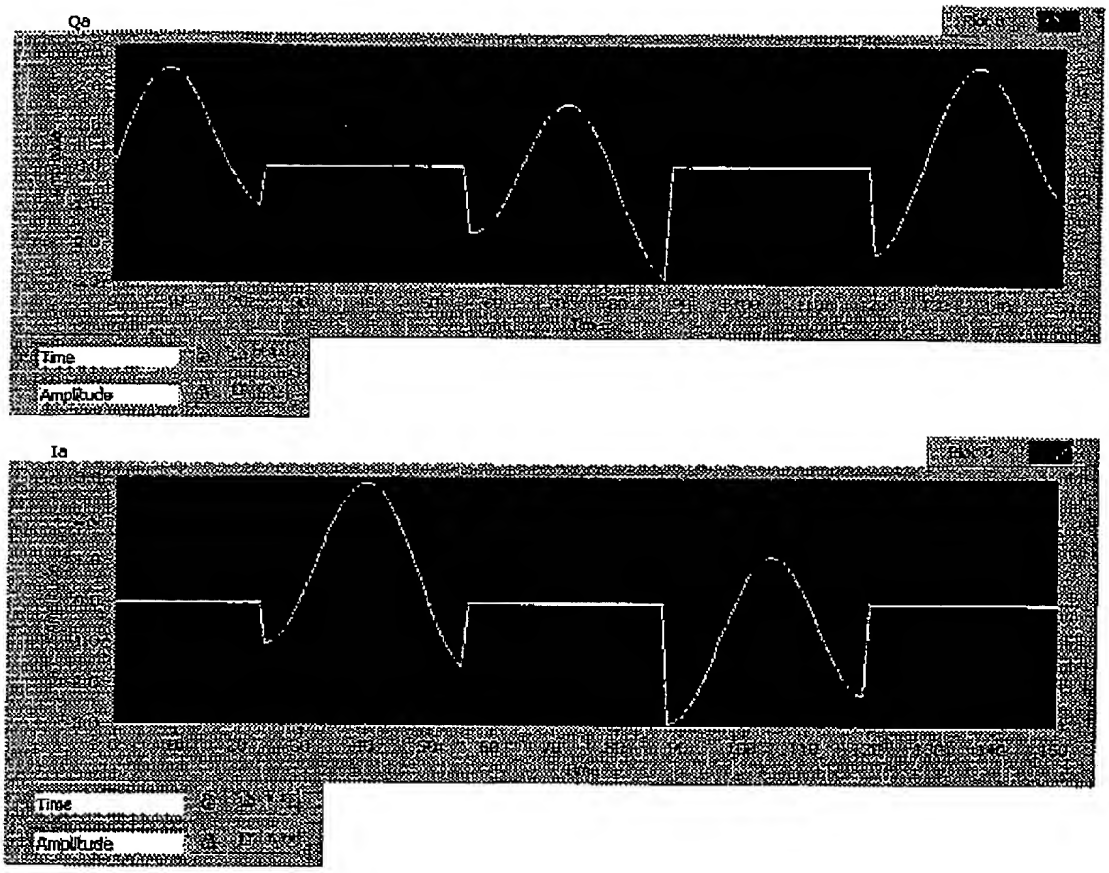
The result is



which is signal 9 in block diagram.

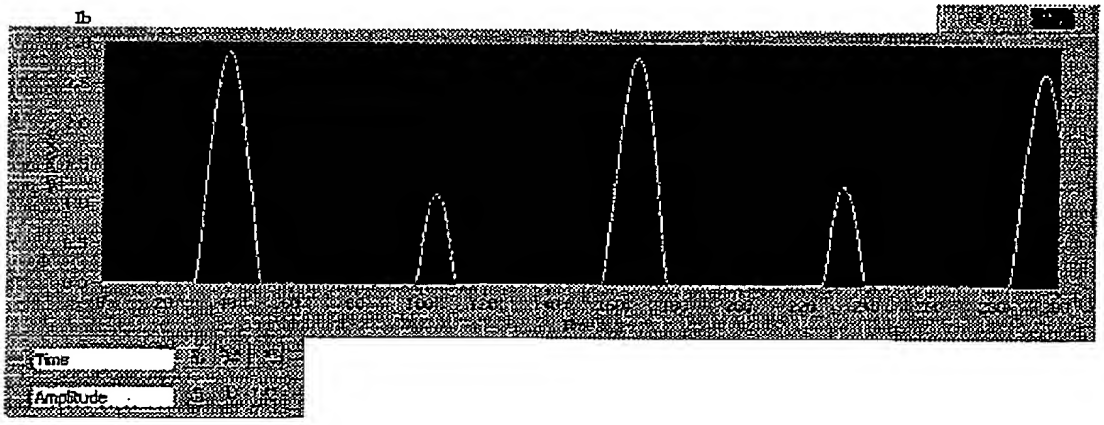
A selector at frequency twice the center frequency selects the I and Q branches.

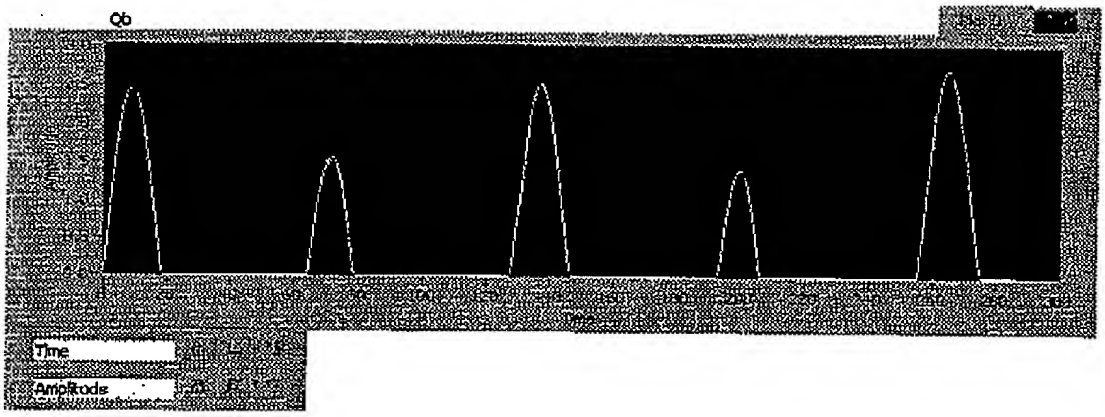
The resulting signals are pictured below



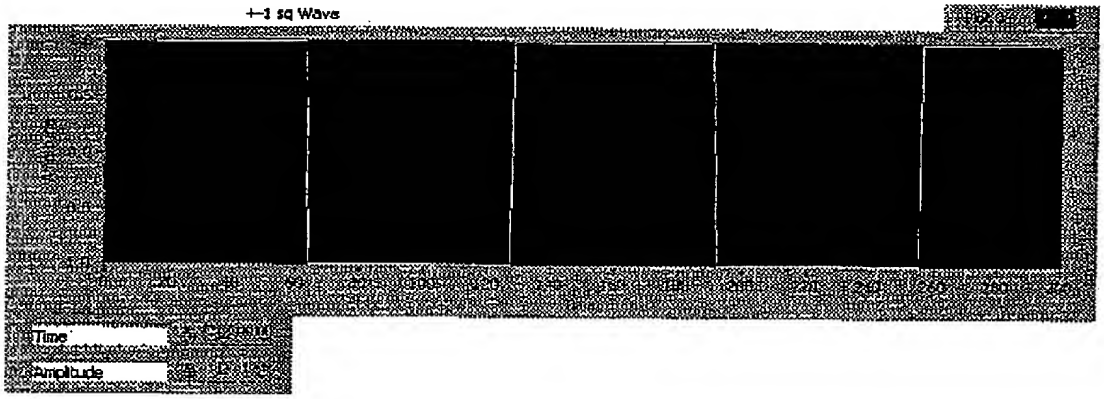
A threshold circuit forces to zero the signal below zero (zero is a level chosen in this example but it is not mandatory).

Result is in Qb and Ib.

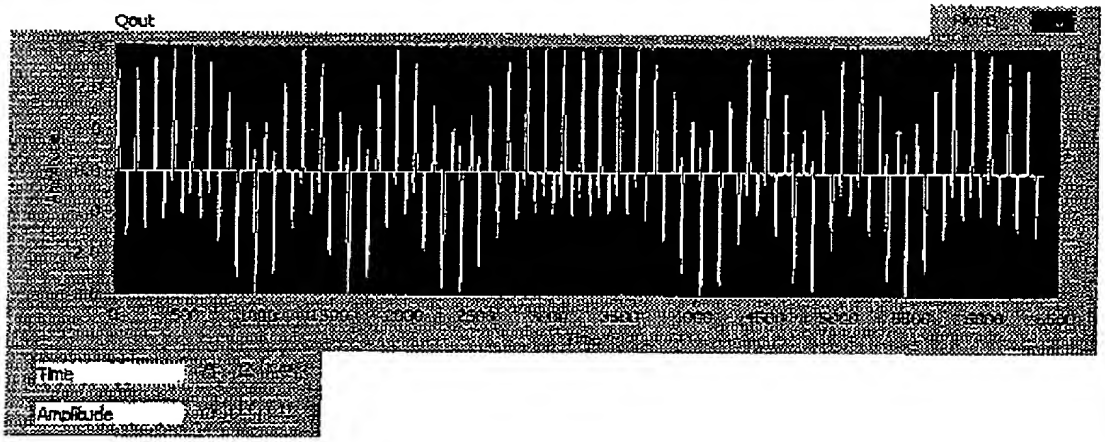


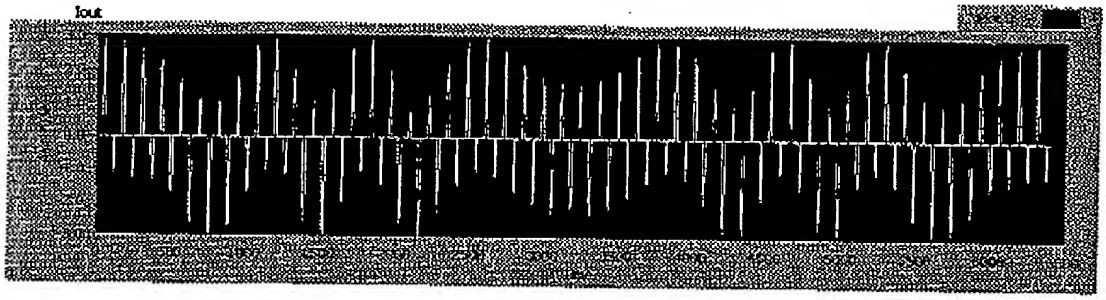


The Qb and Ib signals are multiplied by a square wave at carrier frequency.

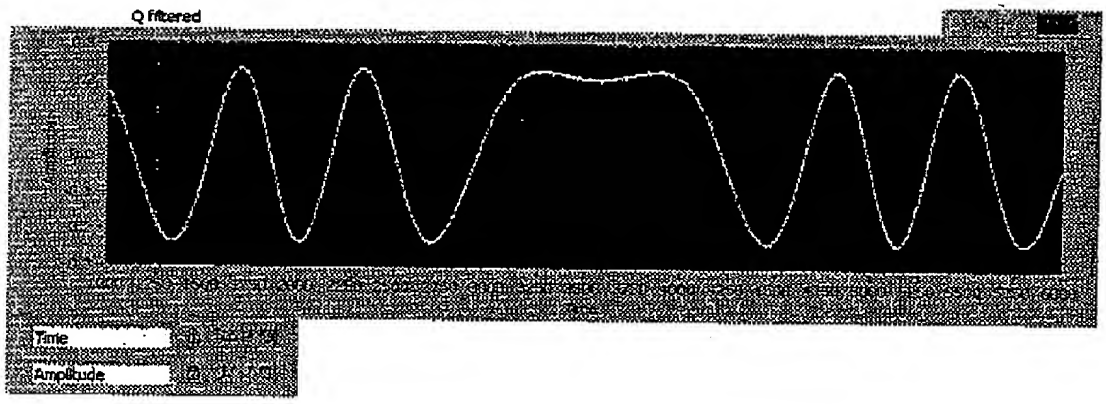


The results are Iout and Qout waveforms.





To better evaluate from the picture the effective quadrature of the signal, a low pass filter is added and the resulting waveform is Ifiltered and Qfiltered.



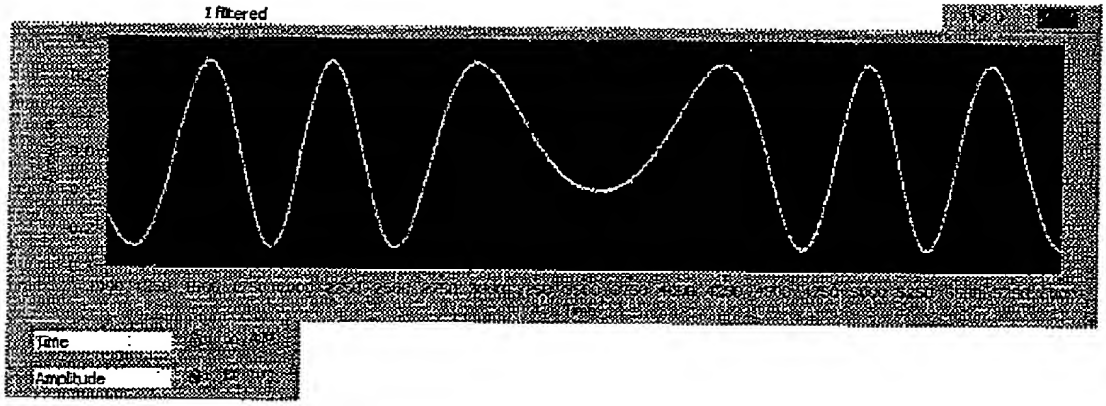
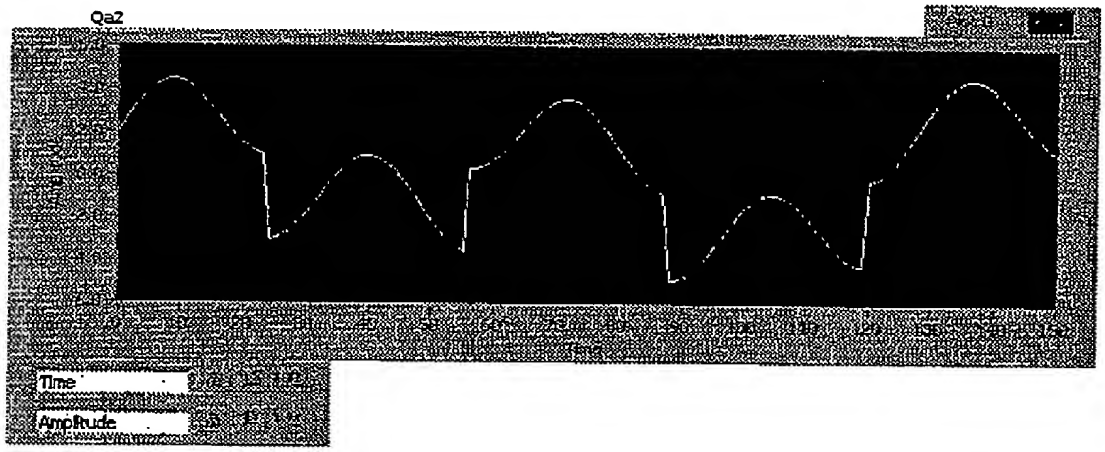


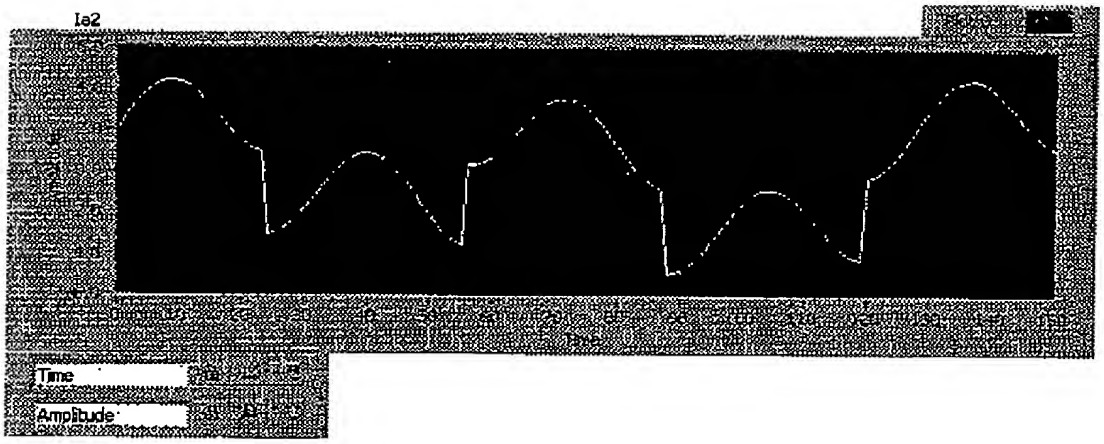
Figure 3

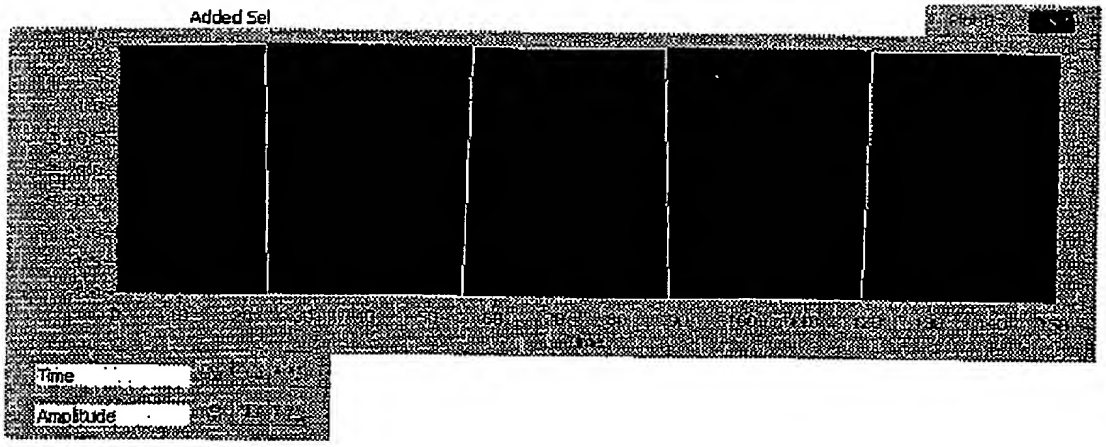
The difference between figures 2 and 3 is the selection process.

The selection process is performed by the mean of the threshold slicer and the addition of a shift of the unwanted part of the signal on each output.

The signal after the 4 FC addition, is added of a square wave at the same frequency of the selection signal.
Result is in Qa2 and Ia2, in this case the selection signal is named Added sel and has amplitude 2.

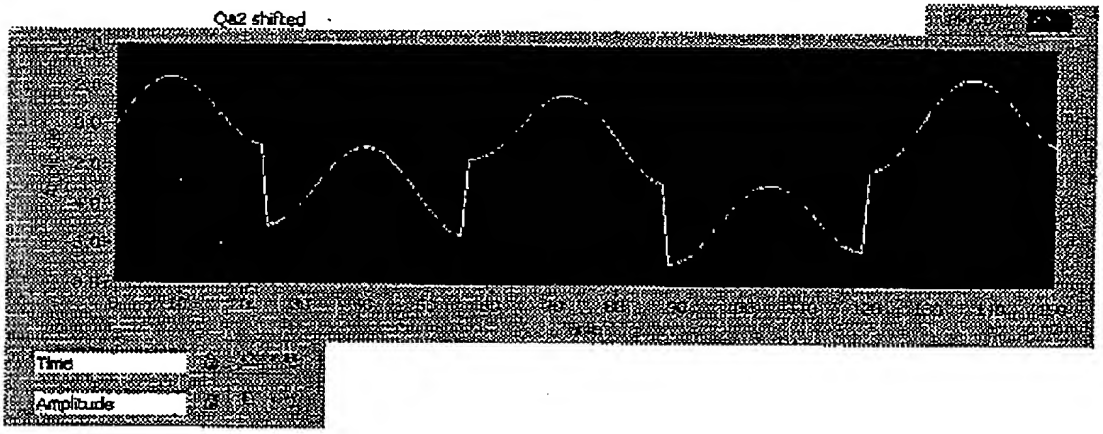


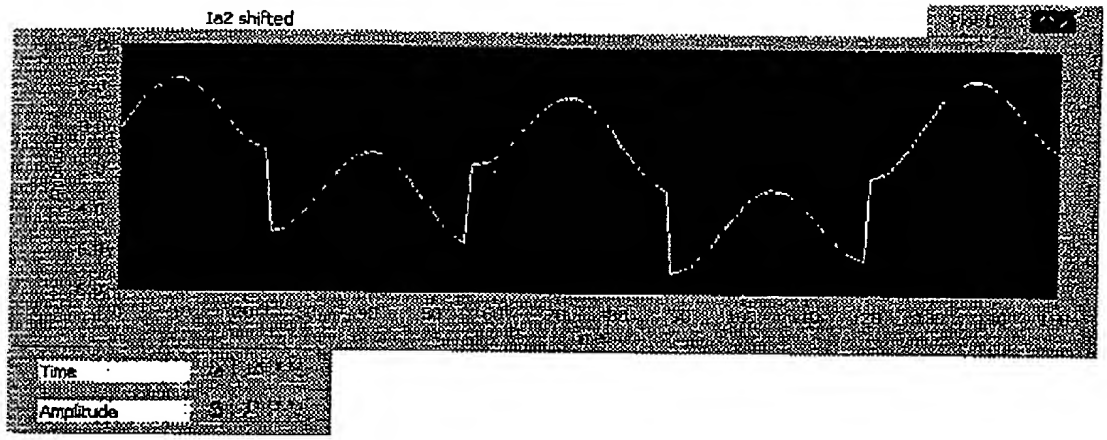




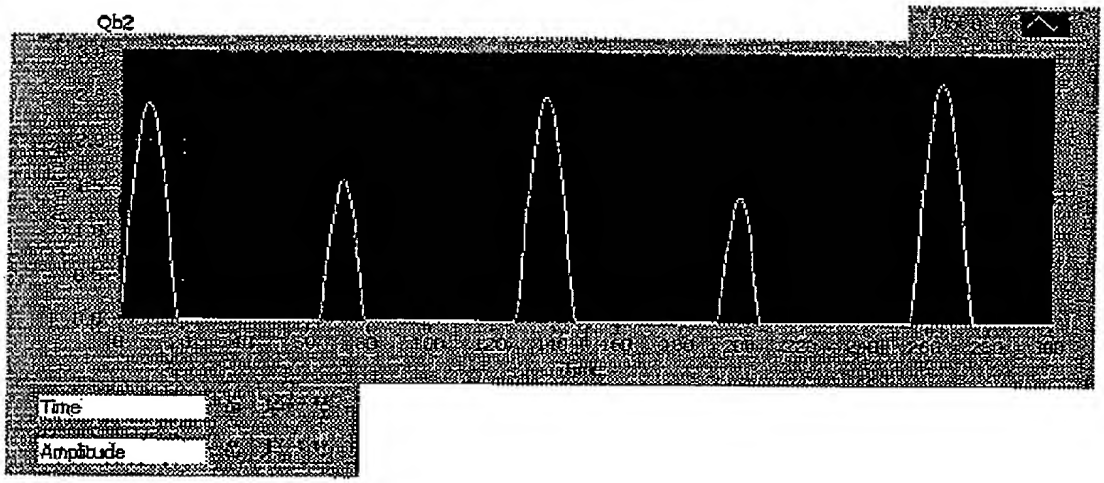
The signal in then shifted by a level of 2; level of added signals and of shifted signal are dependent on system dynamic range and threshold levels.

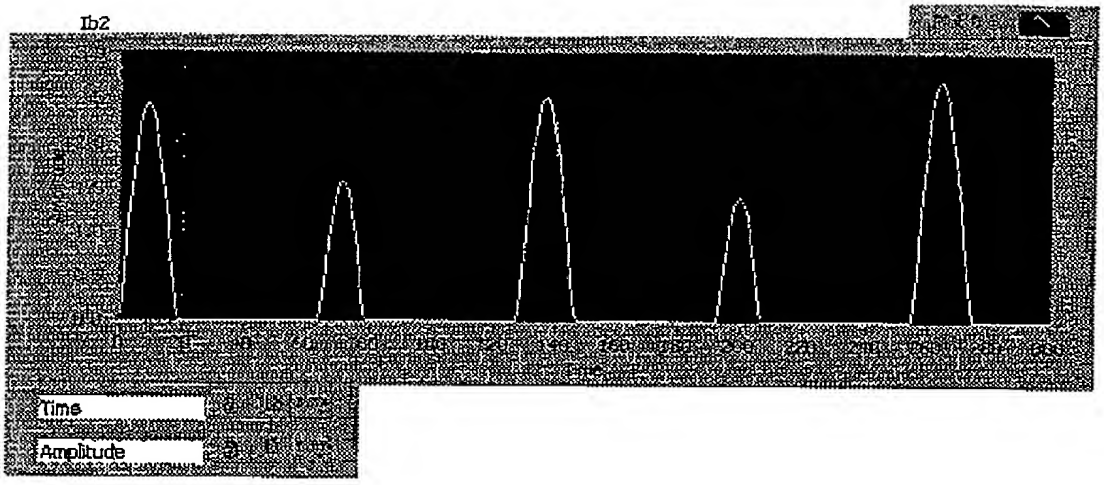
Here are the resulting signals.





After the threshold slicer, we have again the same values as in case of fig 2.





It is believed that the above waveforms could be useful to clarify all the items indicated by the Examiner.

The applicant has also amended the claims to try to overcome the Examiner's rejections under 35 U.S.C. 112.

The applicant is going to contact the Examiner by phone by the end of August to try to discuss the matter and speed up the procedure.

It will be noted that a sincere effort has been made to positively respond to all of the points raised by the Examiner.

While it is believed that the amended claims properly define the present invention, applicant would be open to any suggestion the Examiner may have concerning different claim phraseology which, in the Examiner's opinion, more accurately defines the present invention.

Respectfully submitted,

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Encl.: Labview Diagrams (Two Pages)